WHAT IS CLAIMED IS:

1. An integrated semiconductor device comprising a plurality of semiconductor elements formed in a semiconductor layer and each having a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain,

at least a predetermined part of the drain of one semiconductor element and a predetermined part of the drain of another semiconductor element being different in impurity concentration.

2. The integrated semiconductor device according to claim 1, wherein

said one semiconductor element and said another semiconductor element are different in breakdown voltage.

3. The integrated semiconductor device according to claim 1, wherein

said one semiconductor element has a high breakdown-voltage performance, said another semiconductor element has a lower breakdown-voltage performance than that of said one semiconductor element, and said at least the predetermined part of the drain of said one semiconductor element has an impurity concentration lower than that of said predetermined part of the drain of said another semiconductor element.

4. The integrated semiconductor device according to claim 1, wherein

said another semiconductor element has a breakdown voltage of at most 100 V.

5. The integrated semiconductor device according to claim 1, wherein

said source is located in a surface layer of said semiconductor layer

and said body region encloses said source from the inside of said semiconductor layer.

6. The integrated semiconductor device according to claim 1, wherein

the drain of said one semiconductor element and the drain of said another semiconductor element are each constituted of a drain convergence region including a contact portion located in a surface layer of said semiconductor layer and connected to an interconnection, and a drain drift region of the first-conductivity-type semiconductor having an impurity concentration of the first conductivity type lower than that of said drain convergence region and being formed of said semiconductor layer except for said source, said body region and said drain convergence region.

7. The integrated semiconductor device according to claim 6, wherein

at least one of the drain drift region of the drain of said one semiconductor element and the drain drift region of the drain of said another semiconductor element has, in a portion between said source and said drain convergence region, a drain drift layer containing impurities of the first conductivity type with an impurity concentration higher than that of the drain drift region of said at least one of said one semiconductor element and said another semiconductor element.

8. The integrated semiconductor device according to claim 7, wherein

said plurality of semiconductor elements are classified into a group of semiconductor elements having a breakdown voltage of at least 100 V and a group of semiconductor elements having a breakdown voltage less than 100 V,

for said group of semiconductor elements having a breakdown voltage of at least 100 V, a product $N \cdot d$ is in a range from 0.8 to 1.2E12 cm^{-2} where d indicates a thickness from the bottom to the surface of the drain

drift region and N indicates an impurity concentration of the first conductivity type of the drain drift region and,

for said group of semiconductor elements having a breakdown voltage of less than 100 V, a product N · d is greater than 0.8E12 cm^{-2} where d indicates a thickness from the bottom to the surface of the drain drift region and N indicates an impurity concentration of the first conductivity type of the drain drift region.

9. The integrated semiconductor device according to claim 8, wherein

said product N · d of the drain drift region of a semiconductor element in said group of semiconductor elements having a breakdown voltage of less than 100 V is greater than 1.2E12 cm^{-2}.

10. The integrated semiconductor device according to claim 7, wherein

for all of said plurality of semiconductor elements, a product N · d is at least 0.8E12 cm^{-2} where d indicates a thickness from the bottom to the surface of the drain drift region and N indicates an impurity concentration of the first conductivity type of the drain drift region, regardless of the breakdown voltage.

11. The integrated semiconductor device according to claim 1, wherein

in both of said at least the predetermined part of the drain of said one semiconductor element and said predetermined part of the drain of said another semiconductor element, an impurity concentration is high at a location in a surface layer of said semiconductor layer and the impurity concentration decreases as the location approaches the inside.

12. The integrated semiconductor device according to claim 1, wherein

said semiconductor elements are any of a MOSFET (Metal Oxide

Semiconductor Field-Effect Transistor), an IGBT (Insulated Gate Bipolar Transistor), a bipolar transistor and a diode.

13. A method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer and each having a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain, comprising the steps of:

implanting impurities concurrently into at least a predetermined part of the drain of one semiconductor element and into a predetermined part of the drain of another semiconductor element, an implantation mask being used that includes a portion corresponding to the drain of said one semiconductor element and having a first opening ratio as well as a portion corresponding to the drain of said another semiconductor element and having a second opening ratio different from said first opening ratio; and

annealing said integrated semiconductor device after said step of implanting impurities to diffuse said impurities.

14. The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said one semiconductor element has a breakdown voltage higher than that of said another semiconductor element, and

said implantation mask being used has said first opening ratio smaller than said second opening ratio.

15. The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said one semiconductor element is adjacent to said another semiconductor element, and

said method further comprises the step of providing, in said semiconductor layer, a wall-shaped element-isolation insulating film for isolating said one semiconductor element from said another semiconductor

element, prior to said step of implanting impurities.

16. The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said implantation mask has masking portions and openings in the shape of stripes, and said implantation mask is used by being placed with said stripes arranged in the direction parallel to a carrier path from the source to the drain of said semiconductor elements.

17. The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said implantation mask being used is a mesh implantation mask having dot-like openings dispersed in a masking portion.

18. The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said implantation mask being used is a dot implantation mask having dot-like masking portions dispersed in an opening.